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EXAMINER	
PHAM, CHRYSTINE	
ART UNIT	**PAPER NUMBER**
2192	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/982,020	MARKSTEIN ET AL.	
	Examiner	Art Unit	
	Chrystine Pham	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-27,29 and 31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-27,29 and 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to Amendment filed on March 23rd 2005. Claims 1, 4, 25, 29, and 31 have been amended. Claims 2, 28, and 30 have been canceled. Claims 1, 3-27, 29, and 31 are presented for examination.

Response to Arguments

2. Applicant's arguments with respect to claims 1, 2, 4-16, 18-21, 23-28, 30, and 31 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3-27, 29, and 31are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai (*Sakai*, US 2004/0103410 A1) in view of Gold et al. (*Gold*, US 2002/0184473 A1).

Claim 1

Sakai teach a method of allocating registers when compiling source code (see at least *program conversion, compiler* paragraph [0044]; *program conversion apparatus 2, source program 1* FIG.1 & associated text), said method comprising steps of:

- translating source code to intermediate code (see at least *source program, program conversion apparatus, intermediate program, intermediate terms* paragraphs [0046]-[0047]; *syntax analysis apparatus 10* FIG.1 & associated text);

- identifying an operand from said intermediate code (see at least *register allocation, physical register, intermediate term, variable, operand* paragraph [0098]; paragraph [0153]; paragraph [0179]) to store in a real register (see at least *register allocation section 22* FIG.2 & associated text); and
- selecting a class of real registers operable to store said operand (see at least paragraphs [0182]-[0183]).

Sakai does not expressly disclose selecting at least one subclass of said selected class of real registers, wherein said at least one subclass includes a register to store said operand.

However, *Gold* discloses selecting at least one subclass of real registers (see at least *recycling the physical register assignments* paragraph [0010]), wherein said at least one subclass includes a register to store said operand (see at least *first structure, available physical registers* paragraph [0011]). *Sakai* and *Gold* are analogous art because they are directed to register allocation. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of *Gold* into that of *Sakai* for the inclusion of selecting at least one subclass of a selected class of register. And the motivation for doing so would have been to enable tracking, and regulating (i.e., recycling) the physical register assignments (see *Gold* paragraphs [0001]-[0009]).

Claim 3

The rejection of base claim 1 is incorporated. *Sakai* further teaches wherein said selected class includes one of a callee-saved class (i.e., in response to said operand including at least one of local variables, stack items and parameters input by a user) (see at least *variables, intermediate terms, intermediate program* paragraph [0046]; *physical registers, r10 to r19* paragraphs [0182]-[0183]) and a caller-saved class (i.e., in response to said operand including a temporary computation) (see at least *physical registers, r20 to r30, arithmetic operation* paragraphs [0182]-[0183]).

Claim 4

The rejection of base claim 1 is incorporated. *Gold* further teaches wherein said step of selecting at least one subclass further comprises steps of:

- selecting a first set of subclasses within said selected class (see at least *physical registers, first structure* paragraphs [0011]-[0012]);
- determining whether a register included in said first set of subclasses is available to store said operand (see at least *physical registers, first structure* paragraph [0011]-[0012]); and
- in response to said register being available, storing said operand in said register (see at least *physical registers, first structure* paragraph [0011]-[0012]).

Claim 5

The rejection of base claim 4 is incorporated. *Gold* further teaches wherein said first set of subclasses includes at least one of non-used-in-current-operation, non-busy, non-live and non-used subclasses (see at least *first structure, second structure, third structure* paragraphs [0011]-[0012]).

Claim 6

The rejection of base claim 4 is incorporated. *Gold* further teaches wherein said step of selecting at least one subclass further comprises steps of:

- selecting a second (or third or fourth) set of subclasses within said selected class in response to said register not being available in said first (or second or third) set of subclasses (see at least FIG.2A, FIG.2B, FIG.3 & associated text);
- determining whether a register included in said second (or third or fourth) set of subclasses is available to store said operand (see at least FIG.2A, FIG.2B, FIG.3 & associated text); and
- in response to said register in said second (or third or fourth) set of subclasses being available, storing said operand in said register in said second (or third or fourth) set of subclasses (see at least FIG.2A, FIG.2B, FIG.3 & associated text).

Claim 7

The rejection of base claim 6 is incorporated. *Gold* further teaches wherein said second set of subclasses includes at least one of non-used-in-current-operation, non-busy, non-live (see claim 5) and used subclasses (see at least *first structure, second structure* paragraphs [0011]-[0012]).

Claim 8

The rejection of base claim 6 is incorporated. Claim recites limitations, which have been addressed in claim 6, therefore, is rejected for the same reasons as cited in claim 6.

Claim 9

The rejection of base claim 8 is incorporated. *Sakai* further teach wherein said third set of subclasses includes at least one of non-used-in-current-operation, live, and non-busy subclasses (see at least *third structure* paragraphs [0011]-[0012]).

Claim 10

The rejection of base claim 8 is incorporated. Claim recites limitations, which have been addressed in claim 6, therefore, is rejected for the same reasons as cited in claim 6.

Claim 11

The rejection of base claim 10 is incorporated. *Sakai* further teach wherein said fourth set of subclasses includes at least one of non-used in current operation and busy subclasses (see at least *first structure, second structure* paragraphs [0011]-[0012]).

Claim 13

The rejection of base claim 11 is incorporated. *Gold* further teaches storing said operand in a class (i.e., selected other class) other than selected class in response to a register in said fourth set of subclasses not being available (i.e., selected class of registers not including a not-used-in-current-operation register) (see at least FIG.2A, FIG.2B, FIG.3 & associated text).

Claim 14

The rejection of base claim 11 is incorporated. *Gold* further teaches marking said register as used-in-current-operation in response to storing said operand in said register (see at least *second structure* paragraphs [0011]-[0012]).

Claim 15

The rejection of base claim 11 is incorporated. *Gold* further teaches marking said register storing said operand as live and not-used-in-current-operation in response to translating an instruction of said source code (see at least paragraph [0031]).

Claim 16

The rejection of base claim 1 is incorporated. Claim recites limitations, which have been addressed in claim 13, therefore, is rejected for the same reasons as cited in claim 13.

Claim 17

The rejection of base claim 3 is incorporated. Claim recites limitations, which have been addressed in claim 3, therefore, is rejected for the same reasons as cited in claim 3.

Claim 18

Sakai teaches a method of (i.e., a compiler configured to) compiling source code (see at least *program conversion apparatus 2, source program 1* FIG.1 & associated text) comprising steps of:

- generating intermediate code from a portion of source code (see at least *Syntax Analysis apparatus 10* FIG.1 & associated text);
- allocating a plurality of real registers to store a plurality of operands from said intermediate code while generating the intermediate code (i.e., register allocation stage) (see at least *11, 22, 24, 7* FIG.2 & associated text); and

- optimizing stage configured to optimize said intermediate code (see at least *intermediate program, optimization, parallelization* paragraph [0047]; *Parallelization apparatus 11* FIG.1 & associated text; *11* FIG.2 & associated text);
- a final code stage generating machine-readable code from said intermediate code using said plurality of real registers (see at least *program conversion, source program, target program* paragraph [0049]; *Target Program 3* FIG.1 & associated text; *code generation apparatus 12, instruction sequence, target architecture* paragraph [0079]).

Claim 19

The rejection of base claim 18 is incorporated. *Sakai* further teach a plurality of types of operands and said step of allocating further comprises steps of:

- determining a type of operand for at least one of said plurality of operands (see at least *variables, intermediate terms, intermediate program* paragraph [0046]; *physical registers, r10 to r19, r20 to r30, arithmetic operation* paragraphs [0182]-[0183]);
- storing said at least one operand in memory (i.e., selected class of real registers) in response to said operand being a particular type of operand (i.e., selecting a class of registers depending on said type of operand) (see at least *variables, intermediate terms, intermediate program* paragraph [0046]; *physical registers, r10 to r19, r20 to r30, arithmetic operation* paragraphs [0182]-[0183]); and
- allocating a real register (from said selected class of registers depending on said type of said operand) for said operand (see at least *variables, intermediate terms, intermediate program* paragraph [0046]; *physical registers, r10 to r19, r20 to r30, arithmetic operation* paragraphs [0182]-[0183]).

Claim 20

The rejection of base claim 19 is incorporated. *Sakai* further teach wherein said particular type of operand includes a local variable (see at least *variables, intermediate terms, intermediate program*

paragraph [0046]; *variables, intermediate terms, intermediate program* paragraph [0046]; *physical registers, r10 to r19* paragraphs [0182]-[0183]).

Claim 21

The rejection of base claim 19 is incorporated. Claim recites limitations, which have been addressed in claim 19, therefore, is rejected for the same reasons as cited in claim 19.

Claim 22

The rejection of base claim 21 is incorporated. Claim recites limitations, which have been addressed in claim 3, therefore, is rejected for the same reasons as cited in claim 3.

Claim 23

The rejection of base claim 21 is incorporated. Claim recites limitations, which have been addressed in claim 1, therefore, is rejected for the same reasons as cited in claim 1.

Claim 24

The rejection of base claim 23 is incorporated. Claim recites limitations, which have been addressed in claims 5, 7, 9, 11, therefore, is rejected for the same reasons as cited in claims 5, 7, 9, 11.

Claim 25

Claim recites a compiler version performing the method addressed in claim 18, therefore, is rejected for the same reasons as cited in claim 18.

Claim 26

The rejection of base claim 25 is incorporated. Claim recites limitations, which have been addressed in claim 19, therefore, is rejected for the same reasons as cited in claim 19.

Claim 27

The rejection of base claim 26 is incorporated. Claim recites limitations, which have been addressed in claim 20, therefore, is rejected for the same reasons as cited in claim 20.

Claim 29

The rejection of base claim 25 is incorporated. Claim recites limitations, which have been addressed in claim 3, therefore, is rejected for the same reasons as cited in claim 3.

Claim 31

The rejection of base claim 30 is incorporated. Claim recites limitations, which have been addressed in claims 5, 7, 9, 11, therefore, is rejected for the same reasons as cited in claims 5, 7, 9, 11.

5. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Sakai*in view of *Gold* further in view of Grove et al. (*Grove*, US 5659754).

Claim 12

The rejection of base claim 11 is incorporated. *Sakai* and *Gold* do not expressly disclose spilling a register in at least one of said busy and said live subclasses prior to storing said operand in said register in at least one of said busy and said live subclasses.

However, *Grove* discloses spilling a register in at least one of said busy and said live subclasses prior to storing said operand in said register in at least one of said busy and said live subclasses (see at least *80, 88, 86* FIG.4 & associated text; *variables, registers, memory, spill-over, variable, in use only at the beginning of a program, allocation, different variable, remainder of the program, first variable is no longer in use, live variable set, allocation of CPU registers* col.5:10-55). *Grove* and *Sakai* are analogous art because they are both directed to register allocation during optimization of intermediate code. It would have been obvious to one of ordinary skill in the pertinent art at the time the invention was made to incorporate the teaching of *Grove* into that of *Sakai* and *Gold* for the inclusion of spilling a register in

at least one of said busy and said live subclasses prior to storing said operand in said register in at least one of said busy and said live subclasses. And the motivation for doing so would have been to more efficiently utilize/recycle the number of available registers as has been suggested by *Gold* and *Grove* (see *Grove* col.5:10-55).

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chrystine Pham whose telephone number is 571.212.3702. The examiner can normally be reached on Mon-Fri, 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q Dam can be reached on 571.272.3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CP
June 1, 2005

TUAN DAM
SUPERVISORY PATENT EXAMINER